REMARKS

Claims 1-3, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, and 28 are pending in the present application. Claims 4, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, and 29-36 have been withdrawn. By virtue of this amendment, claim 1 has been amended without prejudice or disclaimer of any previously claimed subject matter. Support for the amendment to claim 1 may be found throughout the present application and at least on page 16, lines 2 through 22 and Fig. 1. Amendment or cancellation of certain claims is not to be construed as a dedication to the public of any of the subject matter as previously claimed.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

Allowable Subject Matter

Applicant thanks the Examiner for the indication of allowable subject matter in paragraph numbers 7 and 8 of the Office Action, specifically, that claims 10, 18, 22, 24, and 28 would be allowable if rewritten to overcome the rejections under 35 U.S.C. § 112 and to include the limitations of any base claims and intervening claims. In view of the amendment and remarks below it is submitted that the claims are now in a condition for allowance.

Rejections under 35 U.S.C. § 112, Second Paragraph

The Office has rejected claims 1-3, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26 and 28 under 35 U.S.C. § 112, second Paragraph as being indefinite.

With regard to the second paragraph on page 2 of the Office Action, Applicant has amended claim 1 as indicated above. In particular, Applicant has amended lines 3-5 of claim 1 to more clearly recite "a gate terminal fabricated on a channel region which receives a first input signal, wherein the channel region is formed between said source region and drain region and

[receives the first input signal through a gate insulating film]." As clearly indicated in Fig. 1 and described at least on page 16, lines 2-22 of the application, the first input signal supplied to the gate terminal is transmitted to the gate electrode to influence the channel region through the gate insulating film, e.g., to vary the drain current. Accordingly, no new matter has been added by this amendment.

With regard to the second paragraph on page 2 of the Office Action, Applicant has amended claim 1 as indicated above. In particular, Applicant has amended line 7 of claim 1 to more clearly recite "said well in each of the semiconductor elements is provided with a substrate terminal which receives a second input signal." (Emphasis added). The amendment is fully supported in Fig. 1 and page 16, lines 2-22 of the present application.

Applicant respectfully submits that the claims are indeed definite and clear. The semiconductor element includes "a pair of a P-type semiconductor element and an N-type semiconductor element," as recited in claim 6 (emphasis added). The pair therefore includes a P-type semiconductor element and an N-type semiconductor element each with a respective source region, source terminal, drain region, and drain terminal. As recited in claim 6, for example, the P-type semiconductor element and the N-type semiconductor element of the pair each include a source terminal. As shown in the specification at least in Fig. 10 and described on pages 26, line 17 to page 27, line 7, a P-type semiconductor element QP and a N-type semiconductor element QN are arranged with the source terminal of the P-type semiconductor element connected to a high potential and the source terminal of the N-type semiconductor element connected to a low potential.

The Examiner further stated "it is also unclear whether the P-type semiconductor element is electrically separated from the N-type semiconductor element in claims 6, 10, 18 and 22." As noted by the Examiner, claim 1 recites that "each of said semiconductor elements is electrically separated from the others," and claim 6 recites that "each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element."

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Therefore, a pair of a P-type semiconductor element and an N-type semiconductor element are electrically separated from other such pairs.

Applicant therefore submits that claims 1, 6, 10, 18, and 22 are definite and request withdrawal of the rejections.

Rejections under 35 U.S.C. 102(b)

Claims 1-3 stand rejected under 35 U.S.C. 102(b) as anticipated by Okumura et al. (Japanese Patent Application No. 08-204110).

Applicant submits that Okumura et al. fail to teach or suggest all of the limitations of claims 1-3. Specifically, Okumura et al. fail to teach or suggest a semiconductor device including a plurality of semiconductor elements wherein "the first and second input signals are different signals that are synchronized with each other," as recited by amended claim 1.

Okumura et al. disclose a semiconductor device wherein the bias power supply 111 is connected to P type silicon base 104, which is the base of NMOS, and bias power supply 112 is connected to N type silicon base 106, which is the base of PMOS. (Okumura et al., paragraph 37). Okumura et al. further disclose reducing the threshold voltage of NMOS to about 0.2 V during active by setting a voltage of, for example, 0.5 V (i.e., a fixed voltage) higher than ground potential and lower than a forward voltage of the P-N junction, for the bias power supply 111. During standby, the threshold voltage of NMOS is increased to about 0.5 V by reducing the voltage of the bias power supply 111 to 0 V (i.e., a fixed voltage). (Okumura et al., paragraph 37, 38). Okamura discloses that a voltage is applied to the P type silicon base to obtain a predetermined threshold in the NMOS, the voltage being a fixed voltage of 0.5 V during active and a fixed voltage of 0 V during standby. These fixed voltages are applied to the P type silicon base not as input signals of various levels, e.g., digital signals, but to obtain a required threshold voltage. The P type silicon base 104, therefore, cannot receive input signals of various levels,

e.g., digital signals, because the threshold voltage varies in response to every input of varying signals and would not operate as described in Okamura et al.

In contrast, the substrate terminal (second input terminal) as recited in the semiconductor device of claim 1 receives not a fixed voltage, but rather an individual input, i.e., "the second input signal." The second input signal may be based on a clock signal or the like and be synchronized with a "first input signal" that is applied to the gate terminal. (see, e.g., page 16, lines 16 - 22 of the specification). Therefore, the second input to the substrate is not a fixed voltage. This enables each of the gate terminal and the substrate terminal to receive an unfixed input signal (e.g., digital signal of high level or low level), thereby realizing a two-input and one-output circuit with a single element.

As discussed above, the P type silicon base of Okumura et al. and the substrate as recited in claim 1 receive different signals and accordingly have different functions. For this and the foregoing reasons, Applicant submits that the Okumara does not disclose or suggest the semiconductor device of claims 1-3.

Applicant therefore requests withdrawal of the rejection.

Rejections under 35 U.S.C. 103(a)

Claims 1-3, 6, 8, and 14 stand rejected under 35 U.S.C. 103(a) as obvious over Chang et al. (U.S. Patent No. 3,865,654) in view of Iwamatsu (Japanese Patent Application No. 07-78885).

Applicant submits that Chang et al. and Iwamatsu do not disclose or suggest the semiconductor device of claim 1 or claims depending therefrom whether alone or in combination. Specifically, Chang et al. do not disclose or suggest a semiconductor device wherein the substrate receives a signal, e.g., a second input signal, or that the gate receives a signal, e.g., a first input signal, wherein "the first and second signals are different signals that are synchronized with each other."

The Office Action states that Chang et al. does not show a gate terminal receiving a first input signal or the wells receiving a second input signal. Further, the combination of Chan et al. and Iwamatsu fail to disclose or suggest a semiconductor device as recited by claim 1. In particular, Iwamatsu discloses applying voltages V_{BG2} and V_{BG1} to wells 2 and 3 respectively. V_{BG2} is a fixed positive voltage and V_{BG1} is a fixed negative voltage, and V_{BG2} and V_{BG1} are used to vary the threshold voltage of the device. A desired threshold voltage cannot be obtained when voltages of various levels are applied to wells 2 and 3. Thus, Chang et al. and Iwamatsu whether alone or in combination fail to disclose or suggest all of the limitations of claims 1-3, 6, 8, and 14.

Applicant therefore requests withdrawal of the rejection.

CONCLUSION

Applicant has, by way of the remarks presented herein, made a sincere effort to overcome rejections and address all issues that were raised in the outstanding Office Action. Accordingly, reconsideration and allowance of the pending claims are respectfully requested. If it is determined that a telephone conversation would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952** referencing docket no. 247322001700. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (Twice Amended) A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel ~~region,~~ region which receives a first input signal, wherein the channel region is formed between said source region and drain region ~~region, which~~ and receives ~~a~~ the first input signal through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others; ~~and~~

said well in each of said semiconductor elements is provided with a substrate terminal which receives a second input signal through a contact hole formed therein at a region other than said source region and drain region; and

the first and second input signals are different signals that are synchronized with each other.